SAMPLE EVIDENCE REPORT

QX-SAMPLE

Open demo board (demo-board.kicad_pcb)

VERDICT
PASS

Board	demo-board.kicad_pcb
Fab profile	JLCPCB standard
Service	Routing + DFM polish
Checked	October 1, 2026
Board size	4 copper layers, 18 footprints, 14 nets, 54 tracks, 16 vias
Report generated	October 1, 2026 by QodeX PCB

Summary

DFM against JLCPCB standard, net connectivity and placement against the board you sent, measured from the delivered file.

CHECK	LIMIT	RESULT
Track width	>= 0.09 mm	PASS
Copper clearance between nets	>= 0.09 mm	PASS
Via drill	>= 0.15 mm	PASS
Plated hole drill	>= 0.2 mm	PASS
Annular ring	>= 0.13 mm	PASS
Copper to board edge	>= 0.3 mm	PASS
Acid traps (acute track junctions)	no junction < 90 deg	PASS
Copper layer count	<= 16 copper layers	PASS
Connectivity: unconnected items	0	PASS
Footprints unchanged (position, rotation, side)	18 of 18	18 / 18
Copper added	-	189.0 mm in 54 tracks, 2 pours
Vias	-	16 added, 16 on the board

Online power-on test

A virtual first power-up of the delivered board: 32 of 32 checks passed, 0 to review, 0 failed.

GROUP	CHECKS PASSED	RESULT
Shorts and connections	6 / 6	PASS
Sources and power budget	4 / 4	PASS
Regulators and converters	3 / 3	PASS
Component ratings	7 / 7	PASS
Protection and safety	5 / 5	PASS
Startup and boot	3 / 3	PASS
Signals between voltage domains	2 / 2	PASS
Copper and heat	2 / 2	PASS

Copper added per layer

LAYER	TRACKS	TRACK LENGTH	POURS	REMOVED
F.Cu	49	174.4 mm	0	-
In1.Cu	0	0.0 mm	1	-
In2.Cu	0	0.0 mm	1	-
B.Cu	5	14.6 mm	0	-

Findings

No findings: every rule above passed on the delivered board.

Differential pairs

Pairs found by name (+/-, _P/_N or P/N suffixes); skew is the difference in routed length.

PAIR	POSITIVE	NEGATIVE	SKEW
USB_CONN_D	USB_CONN_D+ 10.20 mm	USB_CONN_D- 10.20 mm	**0.00 mm**
USB_D	USB_D+ 8.95 mm	USB_D- 9.85 mm	**0.90 mm**

Routed length per net

14 nets on the delivered board, longest first.

NET	ROUTED LENGTH	TRACKS	VIAS	PADS	PAIR
RX	23.01 mm	5	0	2	-
TX	21.27 mm	5	0	2	-
VBUS	20.75 mm	5	0	4	-
GND	17.98 mm	12	10	13	-
+3V3	17.79 mm	6	3	8	-
SWCLK	12.11 mm	3	0	2	-
SWDIO	12.11 mm	3	0	2	-
NRST	11.62 mm	5	2	2	-
USB_CONN_D-	10.20 mm	1	0	2	USB_CONN_D
USB_CONN_D+	10.20 mm	1	0	2	USB_CONN_D
USB_D-	9.85 mm	4	0	2	USB_D
USB_D+	8.95 mm	1	0	2	USB_D
LED	6.95 mm	1	0	2	-
LED_A	6.20 mm	2	1	2	-

What this report covers

Checked automatically

- Every copper item of the delivered file against the JLCPCB standard capability table: track width, copper-to-copper clearance between nets, via and plated-hole drills, annular rings, copper-to-edge distance, acute track junctions and the copper layer count.
- Connectivity: every pad of every net is joined by copper in the delivered file.
- Placement: every footprint of the board you sent is at the same position, rotation and side, with the same content.
- Copper added per layer and routed length per net, measured from the file.

Not checked by this report

- Signal integrity: impedance, crosstalk and return paths are not simulated here; length and skew are geometric only.
- Your own KiCad design rules and net classes beyond the fab table (run KiCad DRC for a sign-off).
- Schematic correctness, part choice, BOM, thermal and EMC behaviour, and the fabricator's own CAM review.

This sample was generated from the open demo board published at https://qodexpcb.com/evidence-library (unrouted -> routed). Customer reports have the same layout.